Reg. No. : ....

Name : ....

Third Semester B.Tech. Degree Examination, December 2015
(2008 Scheme)
08.306 : COMPUTER ORGANIZATION (RF)

Time : 3 Hours

Max. Marks : 100

PART – A

Answer **all** questions.

1. Define bus. Explain briefly on single bus structure.

2. What are assembler directives ? Give examples.

3. Distinguish between auto increment and auto decrement addressing mode.

4. What is the difference between a subroutine and an interrupt-service routine ?

5. Write the sequence of control steps required to add contents of the memory location whose address is at memory location NUM to register R5.

6. What are vectored interrupts ?

7. Discuss about SCSI.

8. State the principle of locality of reference and discuss its importance in memory organization.

9. Define the terms hit rate and miss penalty.

10. What is virtual memory and what are the benefits of virtual memory ?

(10×4=40 Marks)

PART – B

Answer **any one full** question from **each** Module.

Module – I

11. a) Explain briefly on the various types of instruction formats.   10

    b) Illustrate the various addressing modes used by PDP-11 processor with examples.   10

OR

12. a) With a neat block diagram, explain the functional units of a computer.   10

    b) Explain the use of stack and queues.   10

Module – II

13. a) Briefly describe the design of a hardwired control unit.   12

    b) Draw and explain the block diagram of a complete processor.   8

OR

14. a) Explain the sequence of operations needed to perform processor functions :

    i) Fetching a word from memory.

    ii) Perform an arithmetic or logical operation.   8

    b) Explain how interrupt requests from multiple devices can be handled.   12

Module – III

15. a) Explain the terms virtual and physical address. Explain address translation mechanism for converting virtual address into physical address with a neat diagram.   10

    b) Write short notes on EEPROM and RAID.   10

OR

16. Describe the various Cache mapping techniques with diagram. Explain the merits and demerits of each technique.   20